

Figure 1

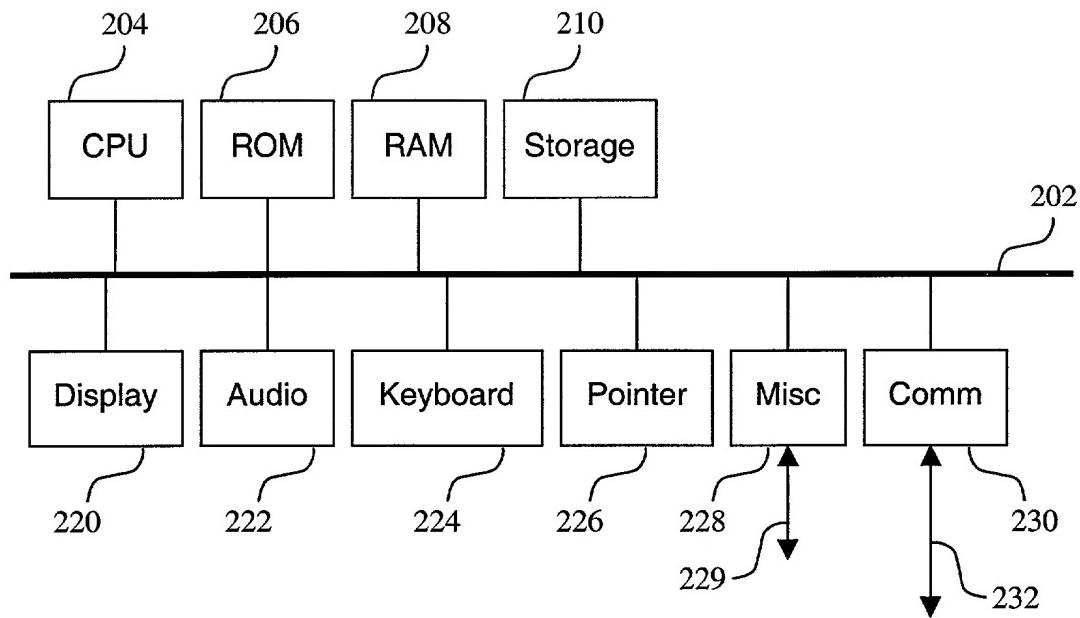


Figure 2

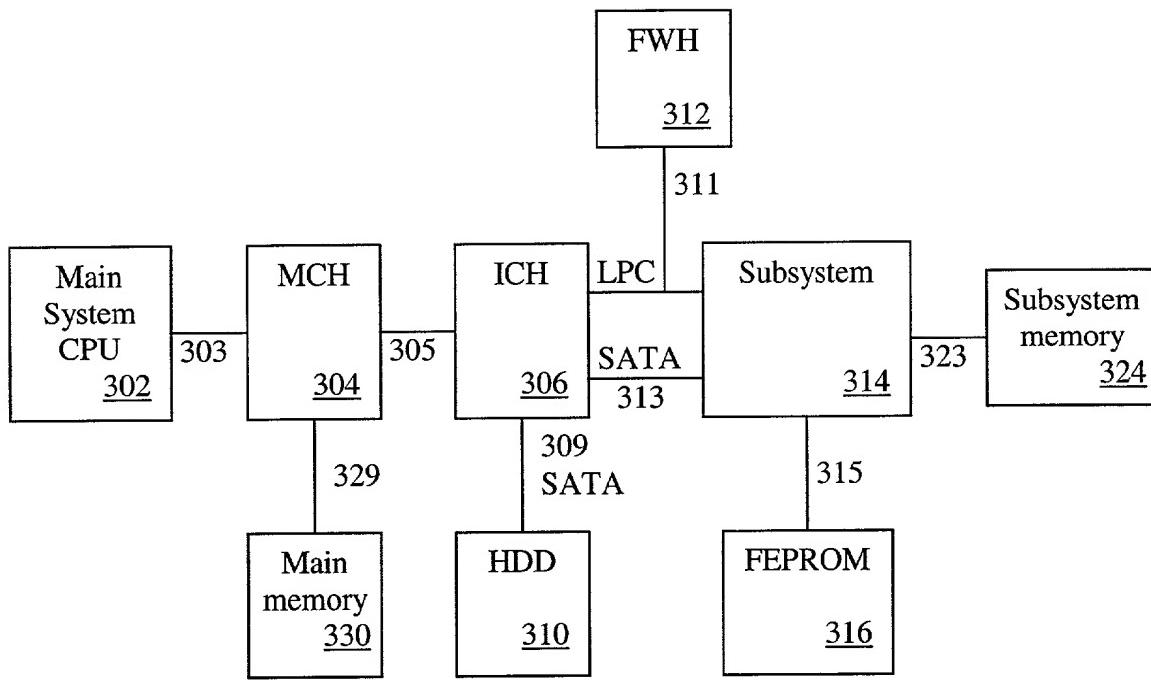


Figure 3

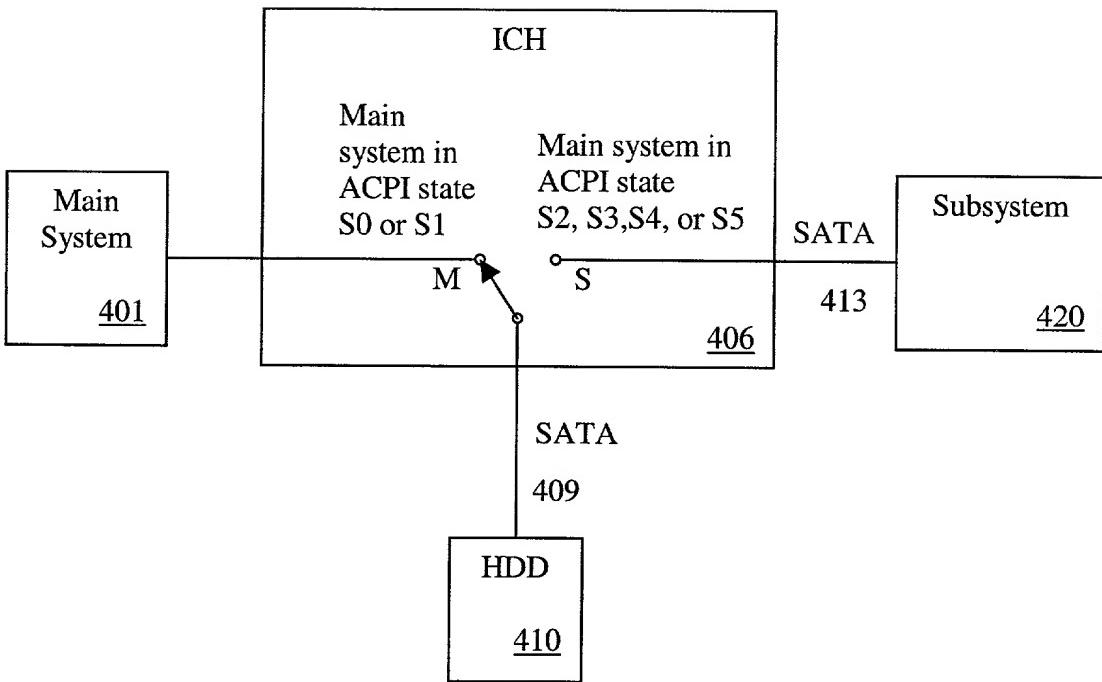


Figure 4

ACPI State	Parallel ATA accessible by:
S0	Main system
S1	Main system
S2	Main system
S3	Subsystem
S4	Subsystem
S5	Subsystem

Figure 5

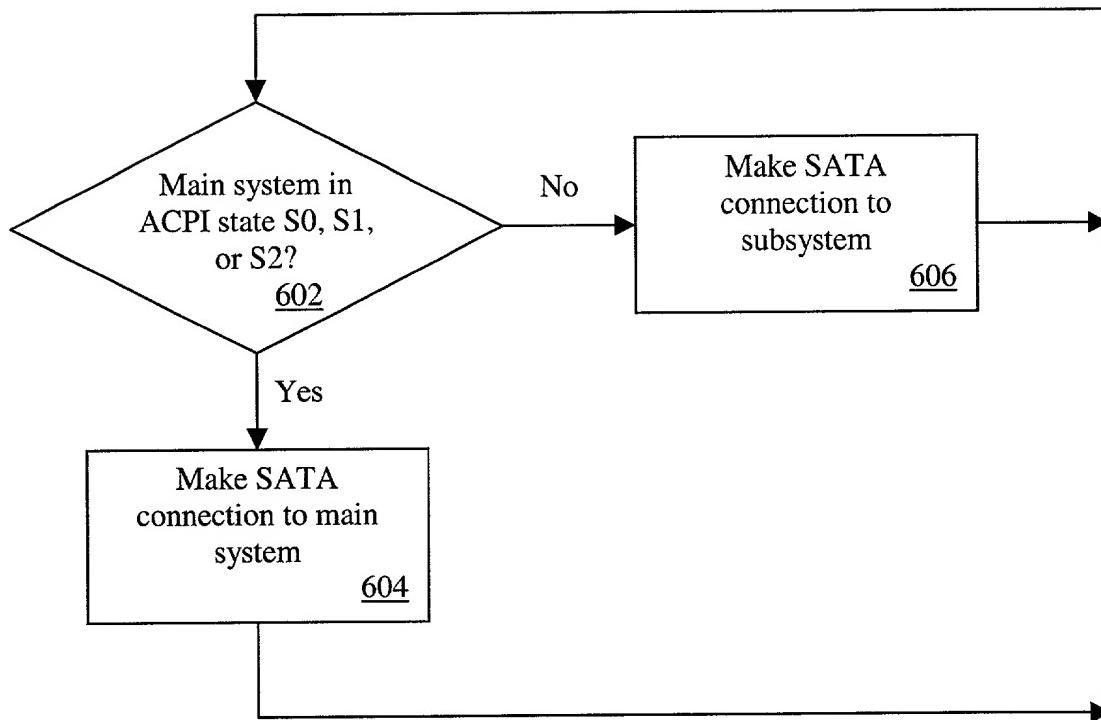


Figure 6

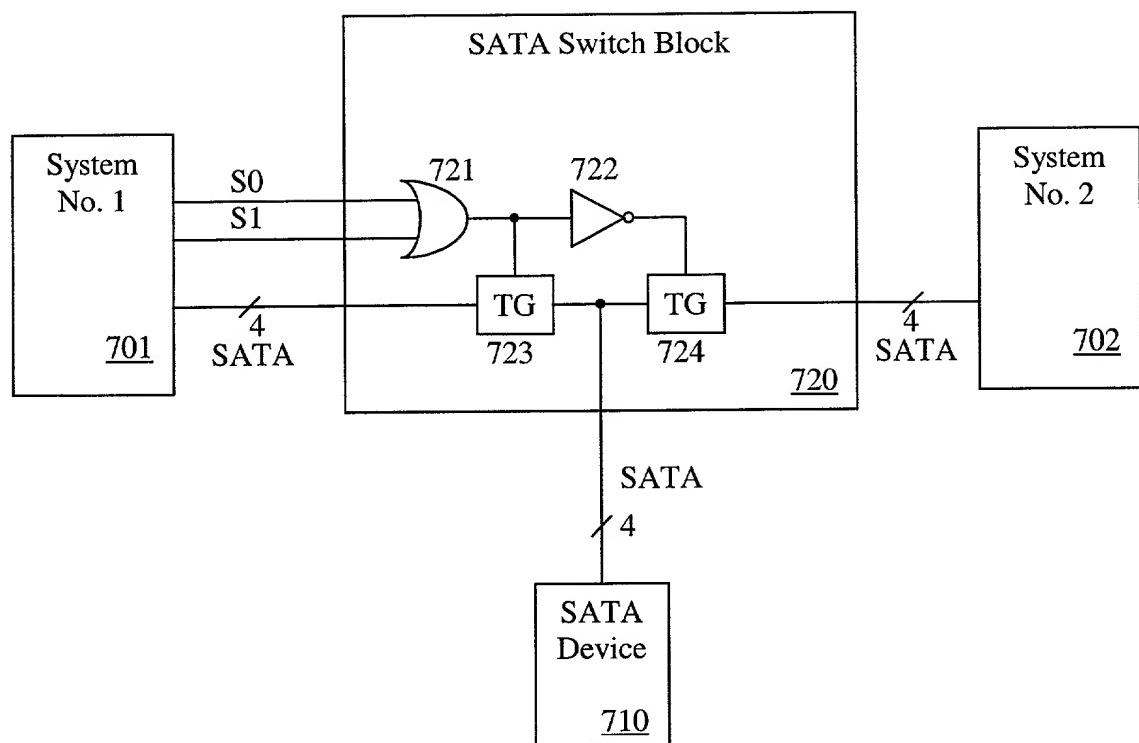


Figure 7